REMARKS

Claims 1-20 are pending in this Application.

Claims 1-20 have been rejected.

No claims have been allowed.

Claim 9 and Claims 15-20 have been amended.

Reconsideration of Claims 1-20, as amended, is respectfully requested.

Claim Objections

On Page 2 of the April 21, 2006 Office Action, the Examiner objected to Claims 15-20 as reciting "computer readable memory." In response, the Applicant has amended Claims 15-20 to recite a "computer readable medium" with "instructions" that direct a computer to operate as an integrated circuit ("IC") simulation system. The Applicant respectfully submits that these amendments place Claims 15-20 in condition for allowance.

On Page 2 of the April 21, 2006 Office Action, the Examiner objected to Claim 9 as being a method claims that recites an apparatus type limitation. In response, the Applicant has amended Claim 9 to recite a method step. The Applicant respectfully submits that this amendment places Claim 9 in condition for allowance.

Claim Rejections Under 35 U.S.C. § 103

On Page 3 of the April 21, 2006 Office Action, the Examiner rejected Claims 1-20 under 35 U.S.C. § 103(a) as being obvious in view of the combination of U.S. Patent No. 5,907,695 to Glenn A. Dearth (hereafter "*Dearth*") and U.S. Patent No. 5,696,771 to Beausang et al. (hereafter "*Beausang*") and U. S. Patent No. 5,841,663 to Sharma et al. (hereafter "*Sharma*"). The Applicant respectfully traverses these rejections for the reasons set forth below.

During *ex parte* examinations of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of non-obviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 USPQ 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781,

783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not be based on an applicant's disclosure. MPEP § 2142.

Applicant respectfully submits that the Patent Office has not established a *prima facie* case of obviousness with respect to the Applicant's invention. The Applicant directs the Examiner's attention to Claim 1 which shows novel and unique features:

> 1. (Original) An integrated circuit ("IC") simulation system operable to (i) store a plurality of Hardware Description Language ("HDL") modules, each one of said plurality of HDL modules representative of a circuit element, (ii) receive a HDL description of a circuit to be simulated, and (iii) synthesize a circuit netlist as a function of said received HDL circuit description and ones of said plurality of HDL modules, said circuit netlist defining behavioral relationships among associated ones of said ones of said plurality of HDL modules, and associate a timing-violation controller with said circuit netlist, said timing-violation controller to ignore selected timing violations sensed during simulation of said circuit as a function of ones of said defined behavioral relationships. (Emphasis added).

The Applicant respectfully submits that the cited prior art, whether taken singly or in combination, does not teach, suggest or even hint at the Applicant's invention.

In the April 21, 2006 Office Action the Examiner stated that, "Dearth, Beausang and Sharma are analogous art because all teach HDL simulation of circuits. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the behavioral relationships in Dearth, and the timing violations of Beausang in the parameterization of Sharma because Dearth teaches a convenient and efficient division of a simulation of circuit (Dearth: column 21, lines 28-30); and Beausang teaches a set of sequential cells that can be scan replaced to just meet the timing and area constraints while offering significant testability for the design (Beausang, column 4, lines 22-25)." (April 21, 2006 Office Action, Page 3, Lines 10-18). The Applicant respectfully traverses this assertion of the Examiner for the reasons set forth below.

In order to establish obviousness by combining references there must be some teaching or suggestion in the prior art to combine the references. *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed.Cir. 1997) ("It is insufficient to establish obviousness that the separate elements of an invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the references."); *In re Rouffet*, 149 F.3d 1350, 1355-56, 47 USPQ2d 1453, 1456 (Fed.Cir. 1998) ("When a rejection depends on a combination of prior art references, there must be some teaching, or motivation to combine the references.")

Evidence of a motivation to combine prior art references must be clear and particular if the trap of "hindsight" is to be avoided. *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed.Cir. 1999) (Evidence of a suggestion, teaching or motivation to combine prior art references must be "clear and particular." "Broad conclusory statements regarding the teaching of multiple

references, standing alone, are not 'evidence.'"). *In re Roufett*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed.Cir. 1998) ("[R]ejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be 'an illogical and inappropriate process by which to determine patentability.'")

The Applicant respectfully submits that the alleged motivation to combine references presented by the Examiner does not meet the legal requirement to establish a finding of *prima facie* obviousness. The Applicant respectfully submits that the alleged motivation to combine references is not clear and particular. The fact that two references are concerned with the same general technical area does not without more provide a "clear and particular" motivation to combine the references. The Applicant respectfully submits that the alleged motivation to combine references has been assumed by "hindsight" in light of the existence of the Applicant's invention.

In particular, the Examiner alleged that a motivation to combine the three references was "because Dearth teaches a convenient and efficient division of a simulation of circuit (Dearth: column 21, lines 28-30)." (April 21, 2006 Office Action, Page 3, Lines 14-16). The Applicant respectfully submits that a general reference to a "convenient and efficient division of a simulation of a circuit" is not a sufficiently "clear and particular" motivation to combine references. The supposed motivation is legally insufficient. The legal insufficiency of the supposed motivation to combine references is supported by the fact that the method and apparatus of *Dearth* addresses only the occurrence of deadlock situations in the bus based networks of

the Virtual Bus Application that described in the *Dearth* reference.

The cited portion of the *Dearth* reference states that "Accordingly, distribution among constituent computers of computer network 450 (FIG. 4) of simulation of bus 104 provides a convenient and efficient division of a simulation of circuit 100 (FIG. 1)." (*Dearth*, Column 21, Lines 28-31). The simulated circuit 100 is a computer network that comprises separately located circuit parts (102A, 102B, 102C) that interact through buses (104, 106). That is, the *Dearth* reference is directed to a method and an apparatus for preventing deadlock situations in a Virtual Bus Application that models complex circuitry using models distributed over a computer network. (*Dearth*, Column 1, Lines 36-39). The problem that the *Dearth* reference addresses is that "the Virtual Bus Application is susceptible to deadlock situations." (*Dearth*, Column 2, Lines 26-28). The simulated circuit 100 is given as an example of a circuit creates deadlock situations. (*Dearth*, Column 2, Lines 26-56).

The deadlock situations described in the *Dearth* reference exist due to the structure and operation of the bus based network of the Virtual Bus Application. The teachings of the *Dearth* reference are not relevant to the Applicant's invention because the Applicant's invention does not have a bus based network structure and does not create the type of bus signals described in the *Dearth* reference and does not create the type of deadlock situations described in the *Dearth* reference.

In any event, there is nothing in the *Dearth* reference that suggests combining the teachings of the *Dearth* reference with the teachings of the *Sharma* reference. There is nothing in

the *Dearth* reference that suggests combining the teachings of the *Dearth* reference with the teachings of the *Beausang* reference. There must be some suggestion or motivation, either in the references themselves, or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. The motivation to create a "convenient and efficient division of a simulation of a circuit" is too general and vague to provide the requisite motivation to modify a reference or to combine reference teachings.

The Examiner also alleged that a motivation to combine the three references was because "Beausang teaches a set of sequential cells that can be scan replaced to just meet the timing and area constraints while offering significant testability for the design (Beausang, column 4, lines 22-25)." (April 21, 2006 Office Action, Page 3, Lines 16-18). The Applicant respectfully submits that a general reference to a "set of sequential cells that can be scan replaced to just meet the timing and area constraints" is not a sufficiently "clear and particular" motivation to combine references. The supposed motivation is legally insufficient. The legal insufficiency of the supposed motivation to combine references is supported by the fact that *Beausang* reference does not teach the Applicant's inventive concept of using a timing-violation controller to ignore selected timing violations that are sensed during simulation of a circuit as a function of defined behavioral relationships.

In rejecting Claim 1, the Examiner cited the *Beausang* reference (Column 35, Lines 31-39) as teaching a timing-violation controller that ignores selected timing violations sensed during simulation of a circuit as a function of defined behavioral relationships. (April 21, 2006 Office

Action, page 4, Lines 5-8). The Applicant respectfully traverses this assertion of the Examiner for the following reasons.

The *Beausang* reference states that "After process 1270 (or its alternative), the fully scan replaced resultant imported netlist is fed in to the normal partial process 1150 with optimization constraints (e.g. timing and area) restored to normal. Partial unscan 1150 then backs off of the scan replacement performed during step 1270 if timing and area violations exist. At the completion of process 1150, a resultant netlist is generated and stored at step 1530. Ideally, at the completion of step 1150, the imported netlist meets given timing and area constraints. As discussed above, timing critical flags can be set with respect to processes 1150 to check for or ignore timing." (*Beausang*, Column 35, Lines 28-39).

This portion of the *Beausang* reference refers to "timing critical flags" being set within step 1150 to check for or ignore timing. A careful reading of the description of step 1150 in the *Beausang* reference reveals that a "timing critical flag" is set to determine whether timing violations should be checked at all through the entire process. The *Beausang* reference states that "Process 1150 starts at logic block 1153 where a timing critical flag (e.g., stored in the input netlist 630) is accessed and checked. The timing critical flag indicates whether or not a user has selected that timing critical constraints should be checked during the subtractive process 1150. At block 1153, if the timing critical flag is not set, then processing flows to logic block 1170 where area constraints are examined, otherwise, processing flows to logic block 1155." (Emphasis added) (*Beausang*, Column 30, Lines 49-56).

It is clear that the *Beausang* reference teaches that the decision whether to check for timing violations is made only once at the beginning of the subtraction process. Either timing violations are checked or they are not checked during the subtraction process. *Beausang* does not teach the concept of selectively ignoring timing violations that are sensed during simulation of a circuit as a function of defined behavioral relationships.

Step 1270 of *Beausang* describes what happens when timing violations are detected during the simulation process. Logic block 1380 of step 1270 (shown in FIG. 23B) determines if timing violations are detected. The *Beausang* reference states that "At logic block 1380, the present invention determines if the worst path of the design copy does not meet timing constraints, e.g., has worse timing than the original design received at block 1310. If this is the case, processing flows to logic block 1400 and the selected unscanned cell is not scan replaced within the original design." (Emphasis added) (*Beausang*, Column 34, Lines 33-38). That is, if there is a timing violation in a cell, then the cell with the timing violation is not used. The cell with the timing violation is not scanned into the original copy of the design (as it otherwise would be in step 1390).

There is no teaching in *Beausang* to ignore the timing violation and go ahead and use a cell that has the timing violation. In *Beausang* all cells with timing violations are discarded. There is no flexibility in *Beausang* to selectively ignore timing violations as taught by the inventive concepts of the Applicant's invention.

In any event, there is nothing in the *Beausang* reference that suggests combining the teachings of the *Beausang* reference with the teachings of the *Sharma* reference. There is nothing

in the *Beausang* reference that suggests combining the teachings of the *Beausang* reference with the teachings of the *Dearth* reference. There must be some suggestion or motivation, either in the references themselves, or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. The fact that a set of sequential cells exists that can be scan replaced to just meet timing and area constraints is too general and vague to provide a supposed requisite motivation to modify a reference or to combine reference teachings.

With respect to Claim 1, the Examiner asserted that it would be obvious to modify *Sharma* with the recitations of *Dearth* and *Beausang* to "associate a timing-violation controller with said circuit netlist (Sharma: column 1, line 24), said timing-violation controller to ignore selected timing violations sensed (Beausang, column 35, lines 31-39) during simulation of said circuit as a function of ones of said defined behavioral relationships (Dearth: column 1, lines 58-60)." (April 21, 2006 Office Action, Page 4, Lines 4-8). However, as previously mentioned, the *Beausang* reference lacks any mention of a timing violation controller that ignores selected timing violations that are sensed during simulation of a circuit as a function of behavioral relationships. Without that showing, the April 21, 2006 Office Action cannot establish that a person skilled in the art would modify *Sharma* with the teachings of *Beausang* as asserted in the April 21, 2006 Office Action.

With regard to the teachings of the cited portion of the *Sharma* reference (Column 1, Line 24), the *Sharma* reference does not teach the concept of associating a timing violation controller with a circuit netlist. The cited portion of the *Sharma* reference simply states that "The object of the present invention is to provide an ASIC synthesizer that synthesizes a circuit

netlist from an HDL circuit description using a library of datapath circuit elements . . . and a library of gate elements."

With regard to the teachings of the cited portion of the *Dearth* reference (Column 1, Lines 58-60), the *Dearth* reference does not teach the concept of ignoring selected timing violations that are sensed during simulation of a circuit as a function of behavioral relationships. The cited portion of the *Dearth* reference simply states that "The behavior of [a] circuit generally includes inter-relationships between various components of the state of the circuit."

For the reasons previously set forth, the Applicant respectfully disagrees with the Examiner's characterization of the *Beausang* system as set forth in the *Beausang* reference. Therefore, even if it were proper (which the Applicant does not admit) to combine the *Beausang* system and the *Sharma* system and the *Dearth* system, the combination of the three references would still not teach, suggest or even hint at the Applicant's invention.

The combination of *Beausang* and *Sharma* and *Dearth* fails to render Claim 1 obvious because, among other things, it fails to teach or suggest the use of a timing violation controller that ignores selected timing violations that are sensed during simulation of a circuit as a function of behavioral relationships.

It is well settled, that while prior art references need not be physically combinable to render obvious an invention under review, obviousness may not be established by combining the teachings of prior art references to provide the claimed invention absent some teaching or suggestion supporting the combination, *i.e.*, the teachings from different references may be combined only if

each reference contains some teaching or incentive to do so. *In re Fritch*, 972 F.2d 1260, 1264, 23 USPQ2d 1780, 1783-1784 (Fed. Cir. 1992); *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). As such, and before a conclusion of obviousness may be made based on a combination of references, a reason, suggestion, or motivation to lead an inventor to combine those references must exist -- if the invention is different from what is disclosed in one reference, but the differences are such that combination with another reference would lead to what is claimed, the obviousness question then requires inquiry into whether there is reason, suggestion, or motivation to make that combination. *Pro-Mold and Tool Co. v. Great Lakes Plastics Inc.*, 37 USPQ2d 1626, 1629-1630 (Fed. Cir. 1996). The combination of the *Beausang* reference and the *Sharma* reference and the *Dearth* reference cannot lead one to arrive at the present invention. There is simply no reason to attempt to combine these references unless one was looking backward at the Applicant's invention.

It cannot be said that one of ordinary skill in the pertinent art would be presumed to know of the teachings of the three references and could solve the same or a similar problem as that the Applicant addresses. *EWP Corp. v. Reliance Universal, Inc.*, 755 F.2d 898, 906-07, 225 USPQ 20, 25 (Fed. Cir.), *cert. denied*, 474 U.S. 843 (1985); *In re* Sernaker, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). The requisite motivation does not stem from any of these teachings, from the perspective of one of ordinary skill in the art, to arrive at the Applicant's invention. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

Claim 1 is not unpatentable under 35 U.S.C. §103(a) over *Sharma* in view of *Beausang* and in view of *Dearth* because, among other reasons, the combination of *Sharma* and *Beausang* and *Dearth* fails to teach or suggest, among other things, the use of a timing violation controller that ignores selected timing violations that are sensed during simulation of a circuit as a function of behavioral relationships. Because the above-emphasized limitations are not disclosed, suggested or even hinted at in the combination of the *Sharma* and *Beausang* and *Dearth* references, they do not render Claim 1 obvious.

Furthermore, dependent Claims 2-7, which depend directly or indirectly from independent Claim 1, contain the limitations contained in Claim 1, as well as any intervening claim. Dependent Claims 2-7 present patentable subject matter over any combination of the *Sharma* and *Beausang* and *Dearth* references.

With respect to the rejection of independent Claim 8 under 35 U.S.C. §103(a) over the *Sharma* reference in view of the *Beausang* reference and in view of the *Dearth* reference, the Applicant notes that independent Claim 8 contains all of the unique and novel limitations of independent Claim 1. The Applicant herein incorporates by reference all of the arguments previously set forth with respect to the obviousness rejections of independent Claim 1. The Applicant respectfully submits that independent Claim 8 is not unpatentable under 35 U.S.C. §103(a) over *Sharma* in view of *Beausang* and in view of *Dearth* because, among other reasons, the combination of *Sharma* and *Beausang* and *Dearth* fails to teach or suggest, among other things, the use of a timing violation controller that ignores selected timing violations that are sensed during simulation

of a circuit as a function of behavioral relationships.

Furthermore, dependent Claims 9-14, which depend directly or indirectly from independent Claim 8, contain the limitations contained in Claim 8, as well as any intervening claim. Dependent Claims 9-14 present patentable subject matter over any combination of the *Sharma* and *Beausang* and *Dearth* references.

With respect to the rejection of independent Claim 15 under 35 U.S.C. §103(a) over the *Sharma* reference in view of the *Beausang* reference and in view of the *Dearth* reference, the Applicant notes that independent Claim 15 contains all of the unique and novel limitations of independent Claim 1. The Applicant herein incorporates by reference all of the arguments previously set forth with respect to the obviousness rejections of independent Claim 1. The Applicant respectfully submits that independent Claim 15 is not unpatentable under 35 U.S.C. §103(a) over *Sharma* in view of *Beausang* and in view of *Dearth* because, among other reasons, the combination of *Sharma* and *Beausang* and *Dearth* fails to teach or suggest, among other things, the use of a timing violation controller that ignores selected timing violations that are sensed during simulation of a circuit as a function of behavioral relationships.

Furthermore, dependent Claims 16-20, which depend directly or indirectly from independent Claim 15, contain the limitations contained in Claim 15, as well as any intervening claim. Dependent Claims 16-20 present patentable subject matter over any combination of the *Sharma* and *Beausang* and *Dearth* references.

The Applicant respectfully submits that the obviousness rejections of Claims 1-20 under 35 U.S.C. § 103 that are set forth in the Office Action of April 21, 2006 have been overcome. The Applicant respectfully submits that Claims 1-20, as amended, are in condition for allowance. Allowance of Claims 1-20, as amended, is respectfully requested.

The Applicant's attorney has made the amendments and arguments set forth above in order to place this Application in condition for allowance. In the alternative, the Applicant's attorney has made the amendments and arguments to properly frame the issues for appeal. In this Amendment, the Applicant makes no admission concerning any now moot rejection or objection, and affirmatively denies any position, statement or averment of the Examiner that was not specifically addressed herein.

SUMMARY

Entry of the amendments in this Response is respectfully requested. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting prosecution of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckbutrus.com*.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS, P.C.

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